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Patent Application

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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A						
	B						
	C						

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	D							
	E							
	F							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
WD	G	Hojat et al.; "AN INTEGRATED PLACEMENT AND SYNTHESIS APPROACH FOR TIMING CLOSURE OF POWER PC MICROPROCESSORS"; 1997; International Conference on Computers and Processors; Austin, Texas, pp. 206-210.
WD	H	Murofushi et al.; "LAYOUT DRIVEN RE-SYNTHESIS FOR LOW POWER CONSUMPTION LSD's"; 1997; Semiconductor DA & TEST Engineering Center DA Development Dept., Kawasaki 210, JAPAN, pp. i-iv.
W	I	Kannan et al.; "A METHODOLOGY AND ALGORITHMS FOR POST-PLACEMENT DELAY OPTIMIZATION"; 1994; Cadence Design Systems, Inc., 2655 Seely Road, San Jose, CA 95134; 31st ACM/IEEE Design Automation Conference, pp. 526-532.
WD	J	Stenz et al.; "TIMING DRIVEN PLACEMENT IN INTERACTION WITH NETLIST TRANSFORMATIONS"; 1997; Siemens AG Semiconductor Group 81617 Munich, Germany, pp. 36-41.
WD	K	Larry Stockmeyer; "OPTIMAL ORIENTATIONS OF CELLS IN SLICING FLOORPLAN DESIGNS"; 1983; Computer Science Department, IBM Research Laboratory, San Jose, CA 95193, pp. 91-101.

Examiner	Date Considered
[signature]	8.8.00

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.